

AO4406
N-Channel Enhancement Mode Field Effect Transistor
General Description

The AO4406/L uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge and operation with gate voltages as low as 2.5V. This device makes an excellent high side switch for notebook CPU core DC-DC conversion. AO4406 and AO4406L are electrically identical.

-RoHS Compliant

-AO4406L is Halogen Free

Features

V_{DS} (V) = 30V

I_D = 11.5A (V_{GS} = 10V)

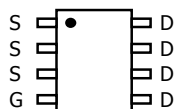
$R_{DS(ON)} < 14m\Omega$ (V_{GS} = 10V)

$R_{DS(ON)} < 16.5m\Omega$ (V_{GS} = 4.5V)

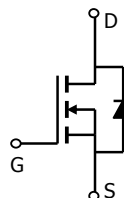
$R_{DS(ON)} < 26m\Omega$ (V_{GS} = 2.5V)

UIS TESTED!

Rg,Ciss,Coss,Crss Tested



SOIC-8


Absolute Maximum Ratings $T_A=25^\circ\text{C}$ unless otherwise noted

Parameter	Symbol	Maximum	Units
Drain-Source Voltage	V_{DS}	30	V
Gate-Source Voltage	V_{GS}	± 12	V
Continuous Drain Current ^{AF}	I_D	11.5	A
$T_A=25^\circ\text{C}$			
$T_A=70^\circ\text{C}$		9.6	
Pulsed Drain Current ^B	I_{DM}	80	
Avalanche Current ^B	I_{AV}	25	A
Repetitive Avalanche Energy ^B L=0.3mH	E_{AV}	94	mJ
Power Dissipation	P_D	3	W
		2.1	
$T_A=25^\circ\text{C}$			
$T_A=70^\circ\text{C}$			
Junction and Storage Temperature Range	T_J, T_{STG}	-55 to 150	$^\circ\text{C}$

Thermal Characteristics

Parameter	Symbol	Typ	Max	Units
Maximum Junction-to-Ambient ^{AF}	$R_{\theta JA}$	23	40	$^\circ\text{C/W}$
$t \leq 10s$				
Maximum Junction-to-Ambient ^A		48	65	$^\circ\text{C/W}$
Steady-State				
Maximum Junction-to-Lead ^C	$R_{\theta JL}$	12	16	$^\circ\text{C/W}$
Steady-State				

Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV _{DSS}	Drain-Source Breakdown Voltage	I _D =250μA, V _{GS} =0V	30			V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =30V, V _{GS} =0V T _J =55°C			1 5	μA
I _{GSS}	Gate-Body leakage current	V _{DS} =0V, V _{GS} = ±12V			100	nA
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} I _D =250μA	0.8	1	1.5	V
I _{D(ON)}	On state drain current	V _{GS} =4.5V, V _{DS} =5V	60			A
R _{DS(ON)}	Static Drain-Source On-Resistance	V _{GS} =10V, I _D =12A T _J =125°C		11.5 16	14 19.2	mΩ
		V _{GS} =4.5V, I _D =10A		13.5	16.5	mΩ
		V _{GS} =2.5V, I _D =8A		19.5	26	mΩ
g _{FS}	Forward Transconductance	V _{DS} =5V, I _D =10A	25	38		S
V _{SD}	Diode Forward Voltage	I _S =10A, V _{GS} =0V		0.83	1	V
I _S	Maximum Body-Diode Continuous Current				4.5	A
DYNAMIC PARAMETERS						
C _{iss}	Input Capacitance	V _{GS} =0V, V _{DS} =15V, f=1MHz		1630	2300	pF
C _{oss}	Output Capacitance			201		pF
C _{rss}	Reverse Transfer Capacitance			142	200	pF
R _g	Gate resistance	V _{GS} =0V, V _{DS} =0V, f=1MHz	0.4	0.8	1.8	Ω
SWITCHING PARAMETERS						
Q _g	Total Gate Charge	V _{GS} =4.5V, V _{DS} =15V, I _D =11.5A	13.5	18	24	nC
Q _{gs}	Gate Source Charge			2.5		nC
Q _{gd}	Gate Drain Charge			5.5		nC
t _{D(on)}	Turn-On DelayTime	V _{GS} =10V, V _{DS} =15V, R _L =1.2Ω, R _{GEN} =3Ω		4	6	ns
t _r	Turn-On Rise Time			5	7.5	ns
t _{D(off)}	Turn-Off DelayTime			32	50	ns
t _f	Turn-Off Fall Time			5	10	ns
t _{rr}	Body Diode Reverse Recovery Time	I _F =10A, dI/dt=100A/μs		18.7	24	ns
Q _{rr}	Body Diode Reverse Recovery Charge	I _F =10A, dI/dt=100A/μs		12.5	15	nC

A: The value of R_{θJA} is measured with the device mounted on 1 in 2 FR-4 board with 2oz. Copper, in a still air environment with T_A=25°C. The value in any given application depends on the user's specific board design.

B: Repetitive rating, pulse width limited by junction temperature.

C: The R_{θJA} is the sum of the thermal impedance from junction to lead R_{θJL} and lead to ambient.

D: The static characteristics in Figures 1 to 6 are obtained using <300 μs pulses, duty cycle 0.5% max.

E: These tests are performed with the device mounted on 1 in 2 FR-4 board with 2oz. Copper, in a still air environment with T_A=25°C. The SOA curve provides a single pulse rating.

F: The current rating is based on the t ≤ 10s junction to ambient thermal resistance rating.

Rev9: May 2011

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TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

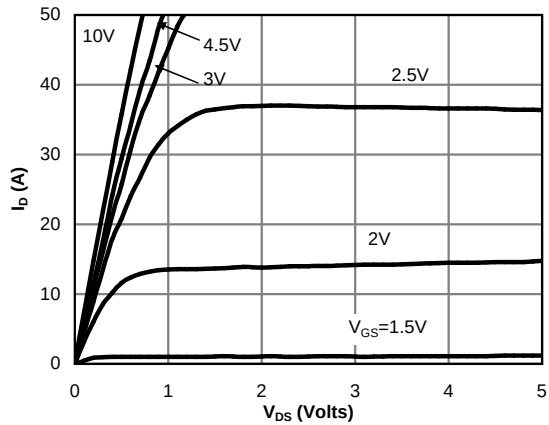


Fig 1: On-Region Characteristics

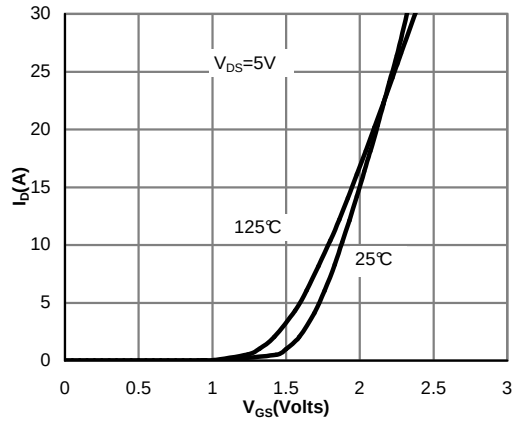


Figure 2: Transfer Characteristics

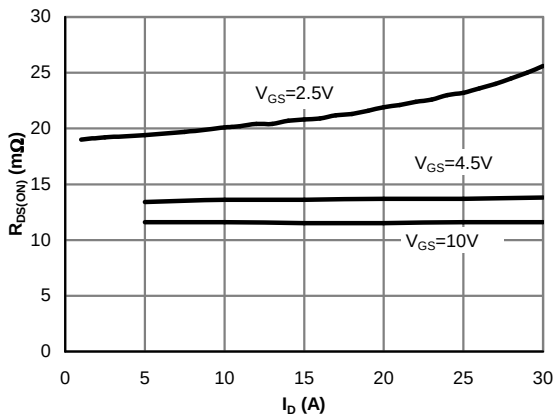


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

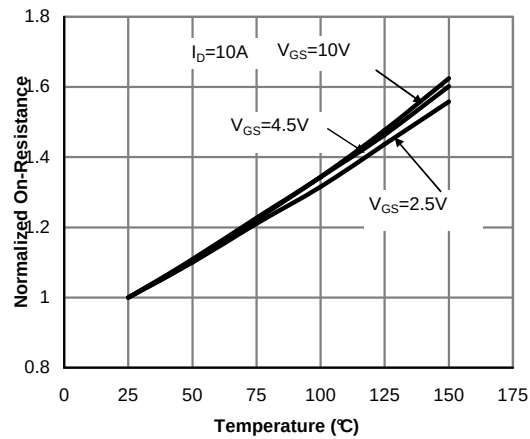


Figure 4: On-Resistance vs. Junction Temperature

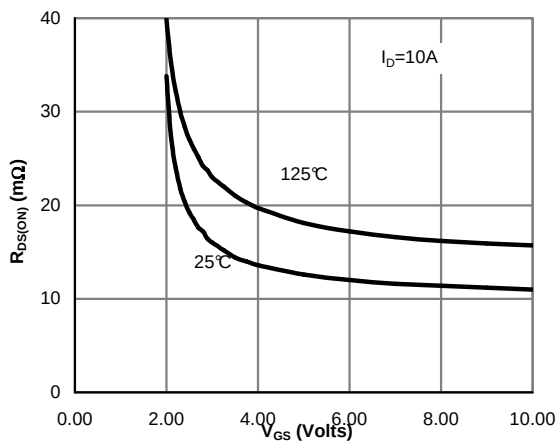


Figure 5: On-Resistance vs. Gate-Source Voltage

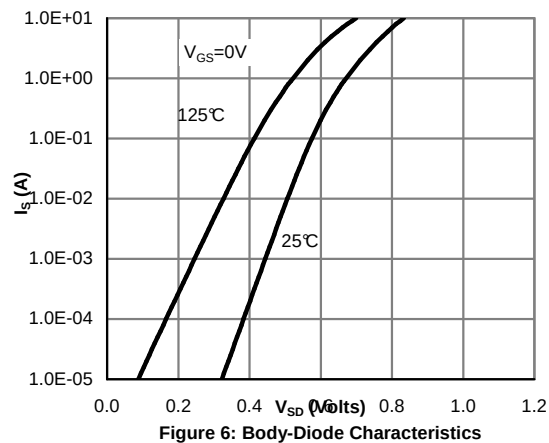


Figure 6: Body-Diode Characteristics

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

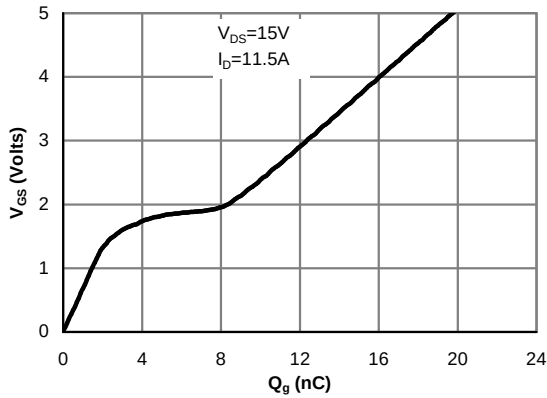


Figure 7: Gate-Charge Characteristics

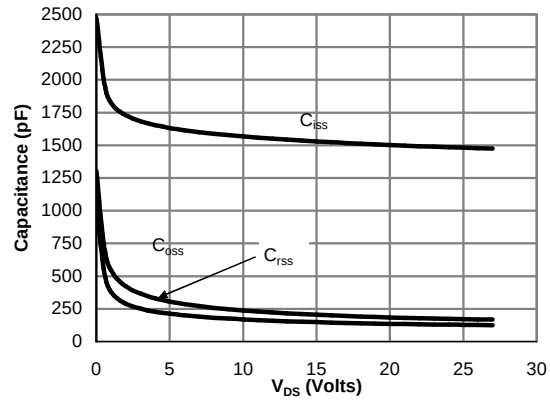


Figure 8: Capacitance Characteristics

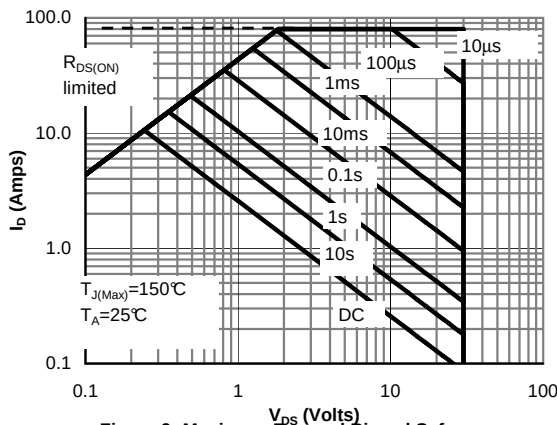


Figure 9: Maximum Forward Biased Safe Operating Area (Note E)

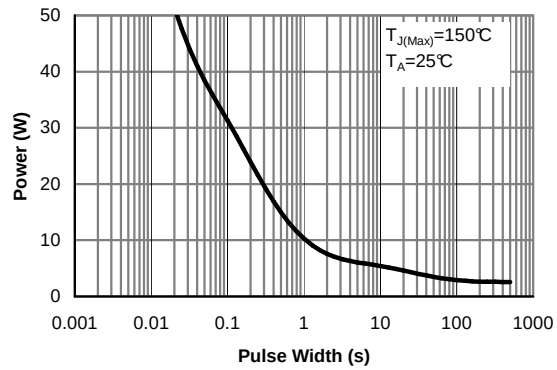


Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note E)

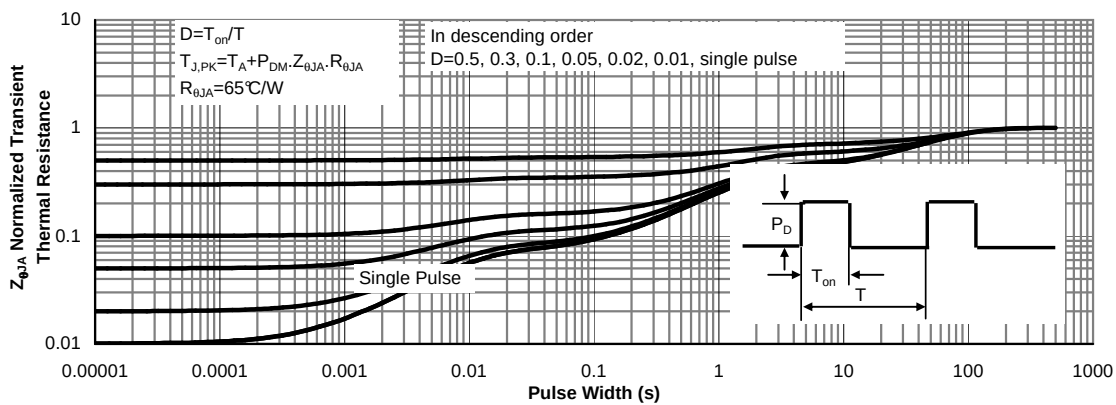


Figure 11: Normalized Maximum Transient Thermal Impedance

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

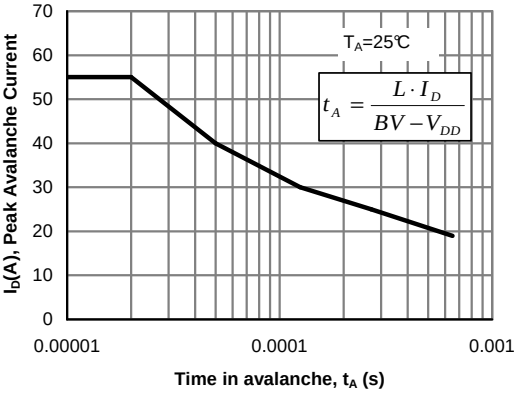


Figure 12: Avalanche capability

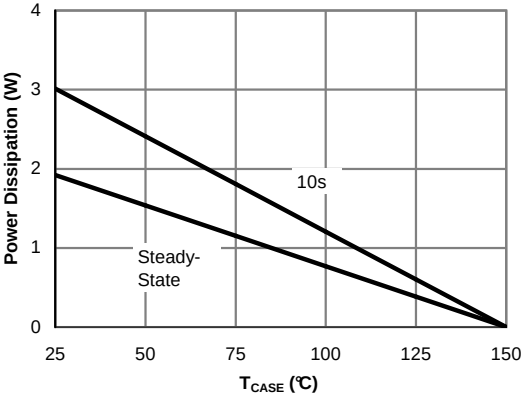
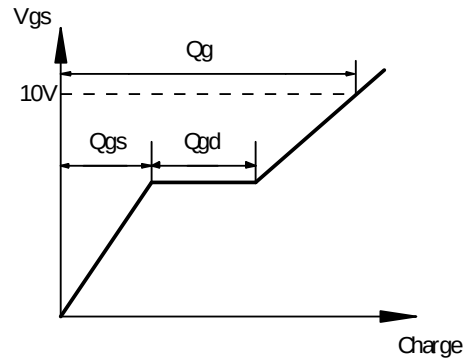
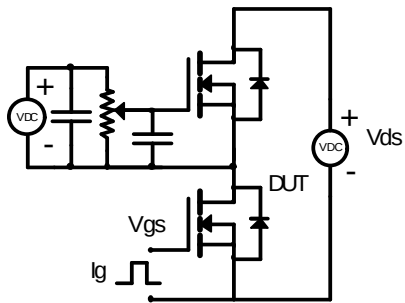
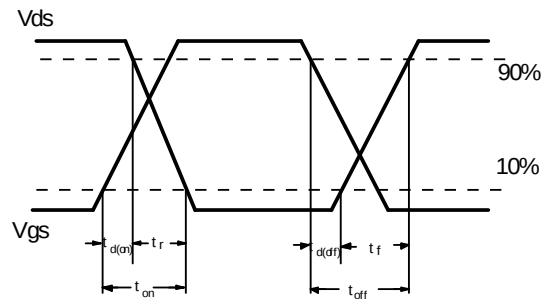
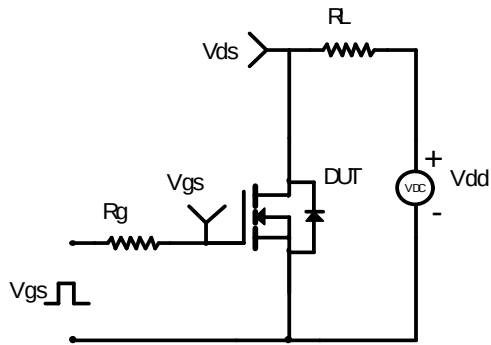


Figure 13: Power De-rating (Note A)

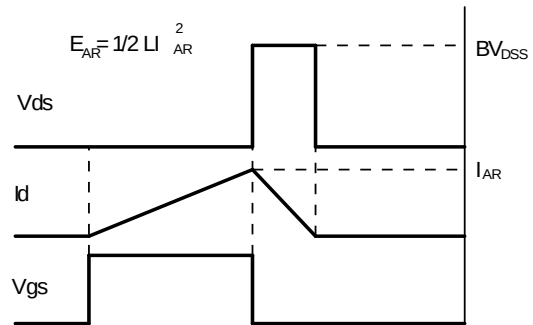
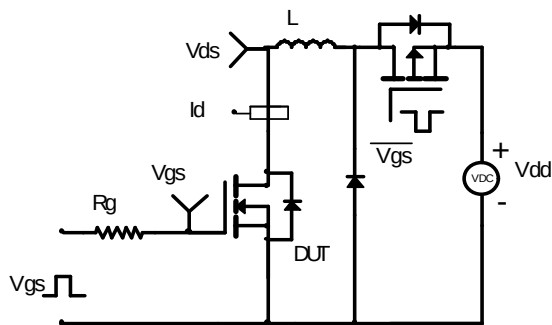
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms

