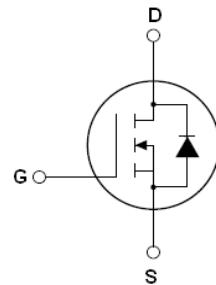
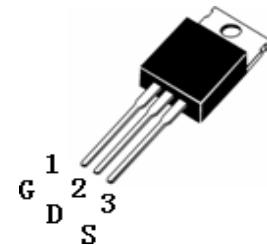


Features:

- Advanced trench process technology
- Special designed for Convertors and power controls
- High density cell design for ultra low R_{dson}
- Fully characterized Avalanche voltage and current
- Avalanche Energy 100% test

ID=80A
BV=80V
 $R_{dson}=6.5\text{m}\Omega$ (Typ.)

Description:

The SSF7509 is a new generation of middle voltage and high current N-Channel enhancement mode trench power MOSFET. This new technology increases the cell density and reduces the on-resistance; its typical R_{dson} can reduce to 6.5mohm.


Application:

- Power switching application

SSF7509 TOP View (TO220)
Absolute Maximum Ratings

	Parameter	Max.	Units
$I_D@T_c=25\text{ C}$	Continuous drain current,VGS@10V	80	A
$I_D@T_c=100\text{C}$	Continuous drain current,VGS@10V	72	
I_{DM}	Pulsed drain current ①	320	
$P_D@T_c=25\text{C}$	Power dissipation	165	W
	Linear derating factor	2.0	W/ °C
V_{GS}	Gate-to-Source voltage	± 20	V
dv/dt	Peak diode recovery voltage	31	v/ns
E_{AS}	Single pulse avalanche energy ②	500	mJ
E_{AR}	Repetitive avalanche energy	TBD	
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to +150	°C

Thermal Resistance

	Parameter	Min.	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-case	—	0.75	—	C/W
$R_{\theta JA}$	Junction-to-ambient	—	—	62	

Electrical Characteristics @ $T_J=25\text{ C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain-to-Source breakdown voltage	80	—	—	V	$V_{GS}=0\text{V}, I_D=250\mu\text{A}$
$R_{DS(on)}$	Static Drain-to-Source on-resistance	—	0.0065	0.008	Ω	$V_{GS}=10\text{V}, I_D=40\text{A}$
$V_{GS(th)}$	Gate threshold voltage	2.0	3.0	4.0	V	$V_{DS}=V_{GS}, I_D=250\mu\text{A}$
g_{fs}	Forward transconductance	—	67	—	S	$V_{DS}=5\text{V}, I_D=30\text{A}$
I_{DSS}	Drain-to-Source leakage current	—	—	2	μA	$V_{DS}=80\text{V}, V_{GS}=0\text{V}$
		—	—	10		$V_{DS}=80\text{V}, V_{GS}=0\text{V}, T_J=150\text{C}$

I _{GSS}	Gate-to-Source forward leakage	—	—	100	nA	V _{GS} =20V
	Gate-to-Source reverse leakage	—	—	-100		V _{GS} =-20V
Q _g	Total gate charge	—	93.6	—	nC	I _D =30A
Q _{gs}	Gate-to-Source charge	—	20.2	—		V _{DD} =30V
Q _{gd}	Gate-to-Drain("Miller") charge	—	33.3	—		V _{GS} =10V
t _{d(on)}	Turn-on delay time	—	17.3	—		V _{DD} =30V
t _r	Rise time	—	15.2	—	nS	I _D =2A, R _L =15Ω
t _{d(off)}	Turn-Off delay time	—	52	—		R _G =2.5Ω
t _f	Fall time	—	19	—		V _{GS} =10V
C _{iss}	Input capacitance	—	3200	—	pF	V _{GS} =0V
C _{oss}	Output capacitance	—	330	—		V _{DS} =25V
C _{rss}	Reverse transfer capacitance	—	260	—		f=1.0MHz

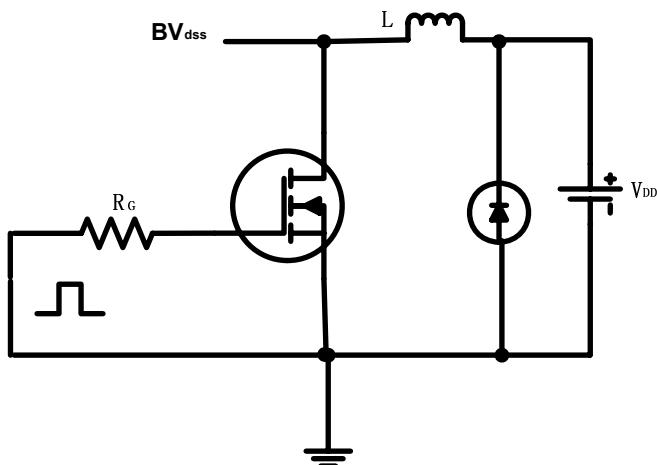
Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Test Conditions
I _S	Continuous Source Current. (Body Diode)	—	—	80	A	MOSFET symbol showing the integral reverse p-n junction diode.
I _{SM}	Pulsed Source Current (Body Diode) ①	—	—	320		
V _{SD}	Diode Forward Voltage	—	—	0.859	V	T _J =25°C, I _S =40A, V _{GS} =0V ③
t _{rr}	Reverse Recovery Time	—	35.9	—	nS	T _J =25°C, I _F =75A
Q _{rr}	Reverse Recovery Charge	—	62.5	—	nC	di/dt=100A/μs ③
t _{on}	Forward Turn-on Time	Intrinsic turn-on time is negligible (turn-on is dominated by L _s + LD)				

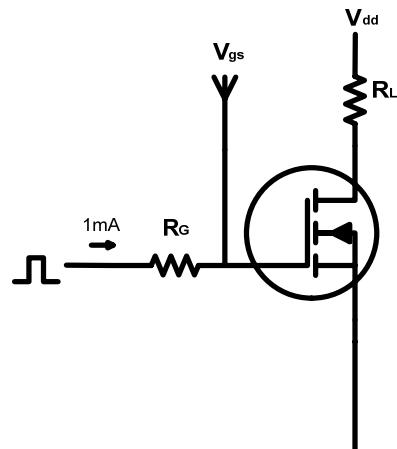
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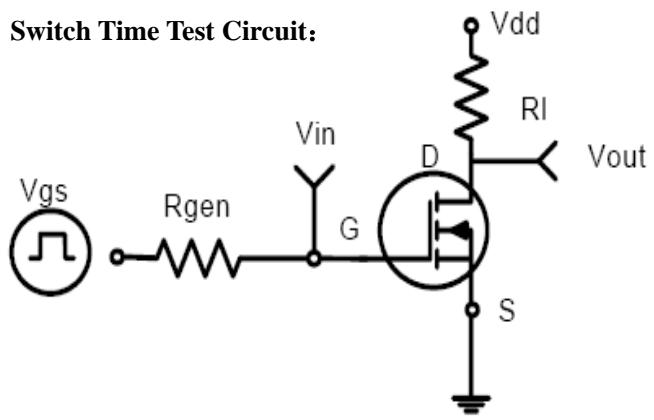
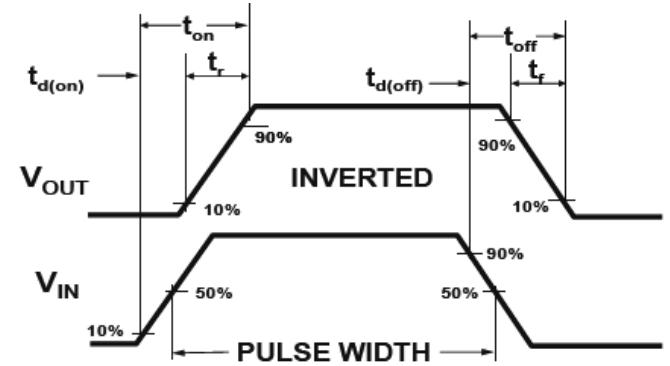
- ① Repetitive rating; pulse width limited by max junction temperature.
- ② Test condition: L = 0.3mH, ID = 57A, VDD = 47V
- ③ Pulse width≤300μS; duty cycle≤1.5% RG = 25Ω Starting TJ = 25°C

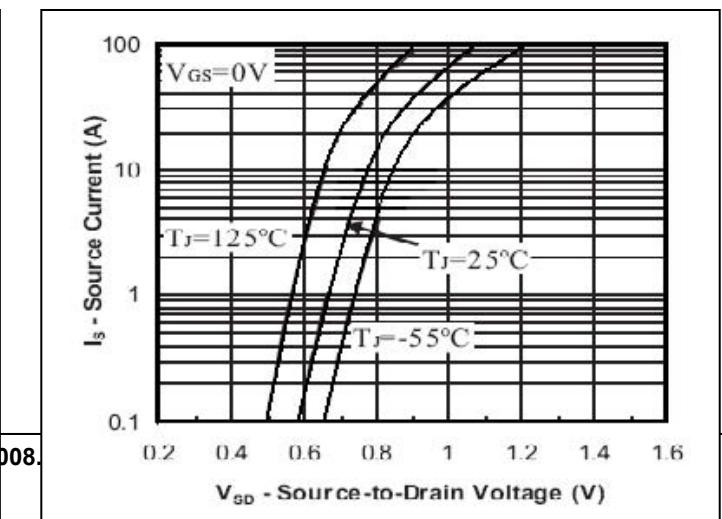
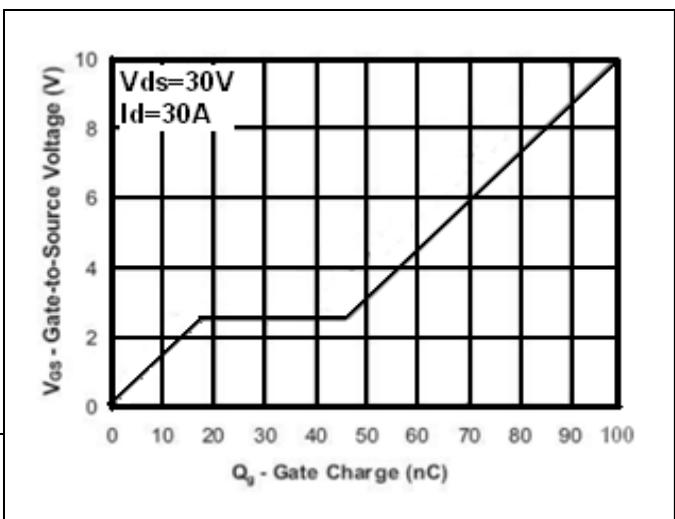
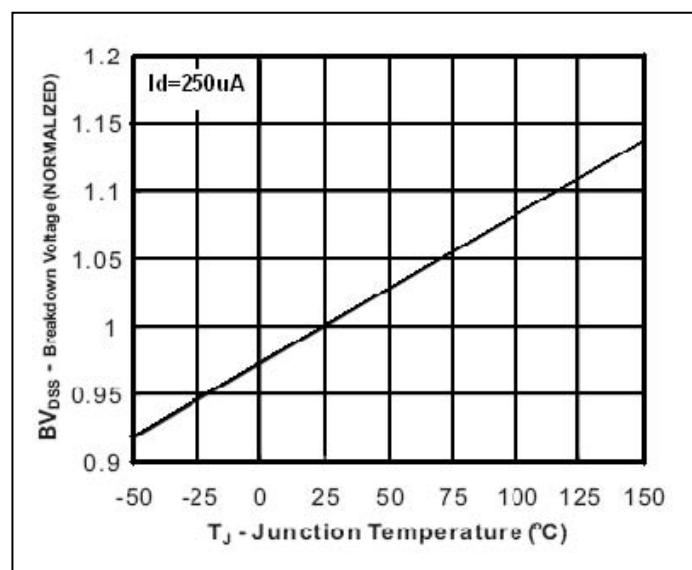
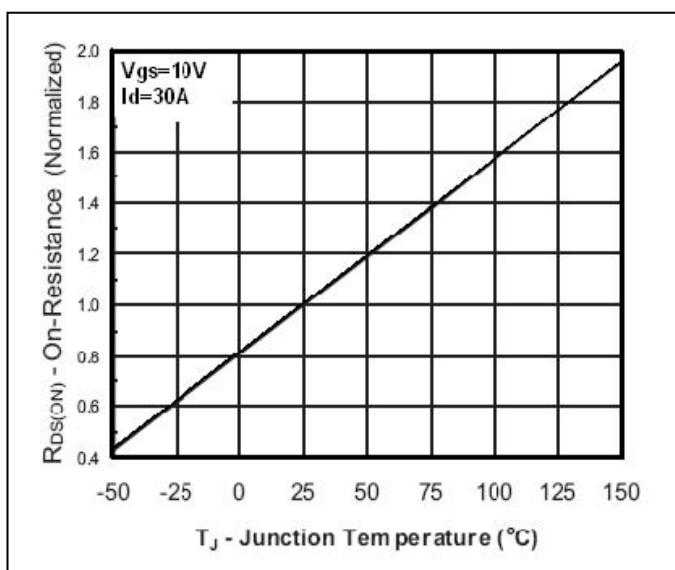
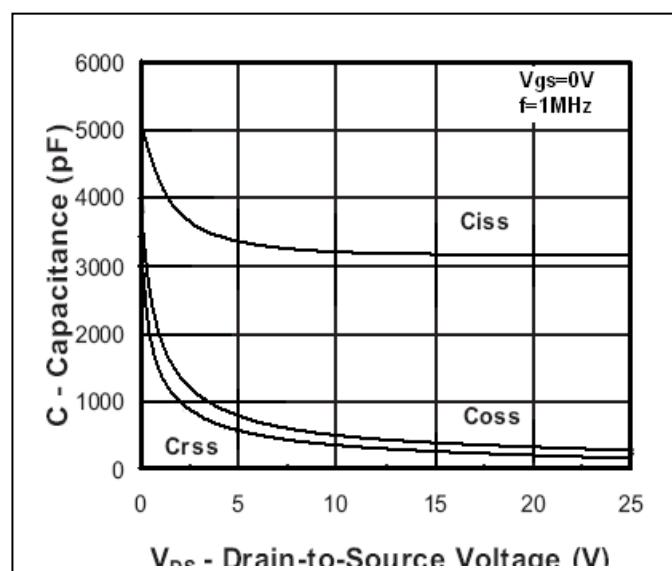
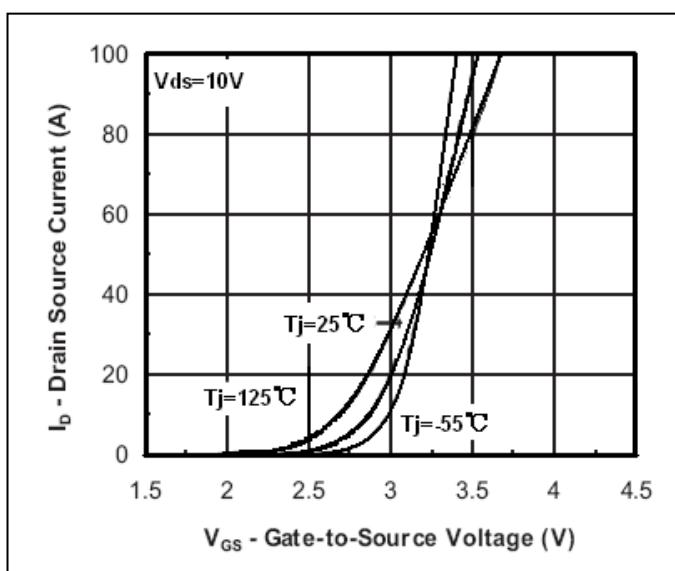
EAS test circuits:

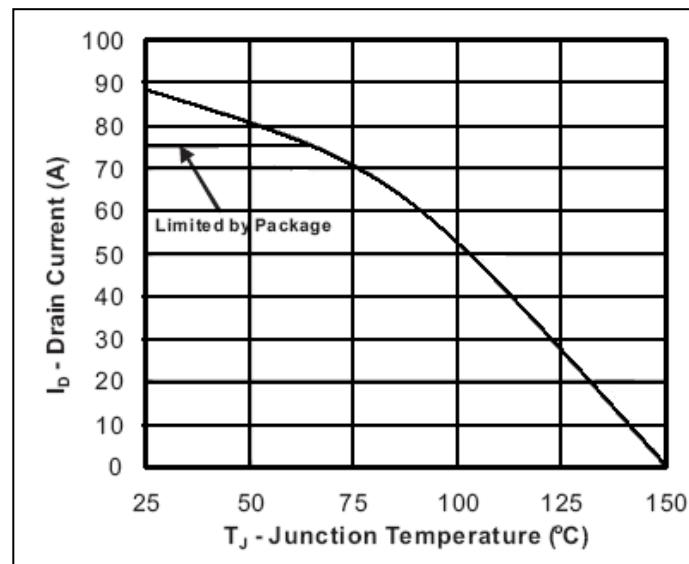
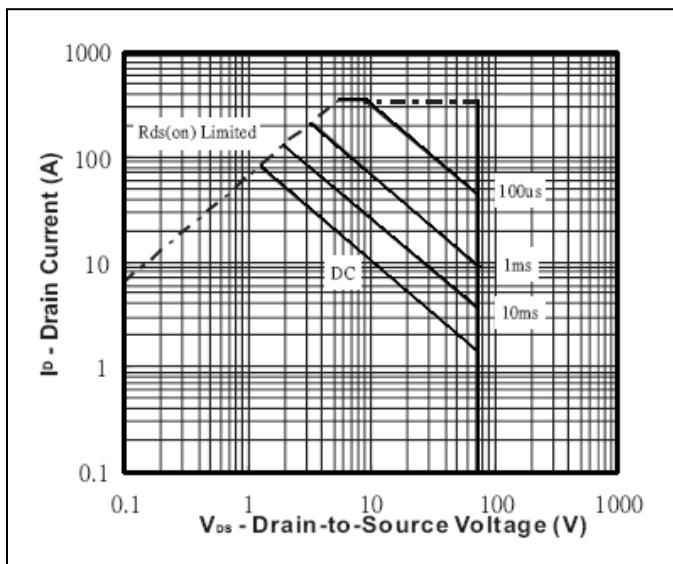


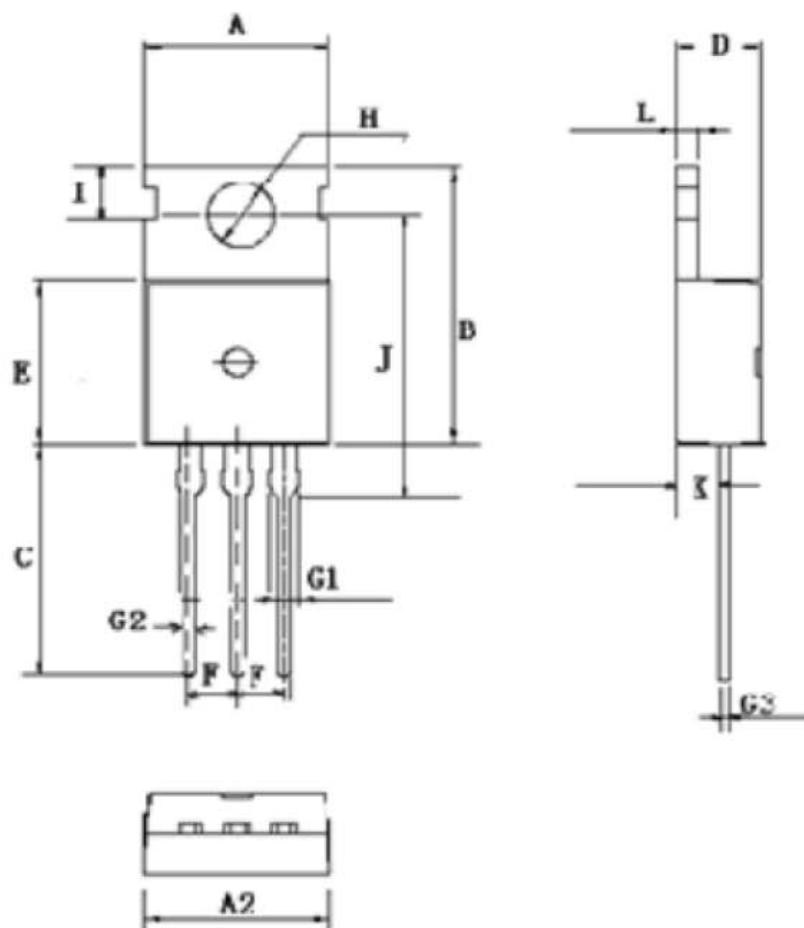
Gate charge test circuit:



Switch Time Test Circuit:

Switch Waveforms:




Source-Drain Diode Forward Voltage

Transient Thermal Impedance Curve
TO220 MECHANICAL DATA:


TO-220 3L

图形对应符号	产品外形尺寸
A(mm)	9.66~10.28
A2(mm)	9.80~10.20
B(mm)	15.6~15.8
C(mm)	12.70~14.27
D(mm)	4.30~4.70
E(mm)	8.59~9.40
F(mm)	2.54 (nom)
G1(mm)	1.42~1.62
G2(mm)	0.70~0.95
G3(mm)	0.45~0.60
H(mm) dia.	3.50~3.70
I(mm)	2.7~2.9
J(mm)	15.70~16.25
K(mm)	2.20~2.90
L(mm)	1.15~1.40
M(mm)	0.5